Microelettronica

Planar Technology for Silicon Integrated Circuits Fabrication
Introduction

- Simplified cross-section of an nMOSFET and a pMOSFET

- Simplified cross-section of a CMOS process with 4 levels of metal
Introduction

• Cross-section of a real 130nm MOSFET

• Cross-section of a real CMOS process
Silicon planar technology: ingredients

**Substrate:** p (or n) type silicon monocrystal

**Doping:**
- Insert donor/acceptors in well-defined areas with a given depth
- Create layers with uniform donor/acceptor concentration

**Interconnections and gates:**
- Metal interconnects
- Inter-metal vias
- MOSFET's gates

**Oxide and other insulators:**
- Thick, inter-layer dielectric (ILD)
- Thin, high-quality gate oxide
- Trench isolation between devices
Photolithography

• Technique used to define geometrical patterns on a semiconductor substrate

• Needed to:
  – dig holes/trenches
  – define shapes by selective etching
  – implant/diffuse dopant
Photolithography

Example: patterning of a window in a SiO$_2$ layer

Step 1: photoresist deposition.
- Photoresist (PR) is an organic polymer sensitive to UV light.
- Positive PR: when exposed to light becomes soluble to PR developer
- Negative PR: when exposed to light becomes insoluble to PR developer
Photolithography

Step 2: photoresist exposure
- PR is selectively exposed to UV light using a mask

Step 3: photoresist development
- PR washed in a developer solution
- Assuming positive PR was used, the portion of PR exposed to UV light in step 2 is dissolved by developer
Photolithography

Step 4: oxide etching
- Chemical etching using HCl
- SiO$_2$ below PR window reacts with HCl and is removed
- PR is insensitive to HCl and protects SiO$_2$
- When SiO$_2$ below PR window is completely removed, reaction stops as Si is insensitive to HCl

Step 5: photoresist removal
- Unexposed PR is removed, leaving the desired patterned oxide
Silicon crystal growth

- Starting material: SiO$_2$
- Highly impure metallurgical Si obtained from:
  $$\text{SiO}_2 + 2\text{C} \leftrightarrow \text{Si} + 2\text{CO}$$
- Then
  (impure) Si + HCl $\leftrightarrow$ SiHCl$_3$, SiCl$_4$ and impurities
Silicon crystal growth

• Then, high purity poly-crystalline Si is produced from trichlorosilane or Si tetrachloride

\[ 2\text{SiHCl}_3 + 2\text{H}_2 \iff 2\text{Si} + 6\text{HCl} \]

1100 °C
Silicon crystal growth

- Si monocrystal ingot grown by Czochralski method

break-up of a poly-crystalline Si bar
Silicon crystal growth

- From poly-crystalline silicon to silicon monocystal ingot
Silicon crystal growth

• Final result:
  – Si monocrystal without defects
  – Ingot of large diameter (up to 12”)
  – high purity (1 part per billion, i.e. $10^{13}$ cm$^{-3}$ impurity on $5 \times 10^{22}$ cm$^{-3}$ silicon atoms)
Silicon wafers production

- Ingots are sliced in thin (0.3 ÷ 1 mm) wafers
- Wafer surfaces are mechanically and chemically polished
Silicon wafers production

Si wafer surface after slicing

Si wafer surface after polishing
Silicon epitaxial growth

- Used to grow a thin layer of single-crystal silicon over a single-crystal silicon substrate

- Advantages
  - improved doping control
  - better bipolar devices
  - prevention of latch-up in CMOS circuits

- Epitaxial growth techniques
  - chemical vapor deposition (CVD)
  - molecular beam epitaxy (MBE)
Chemical vapor deposition (CVD)

- Reactants (gases and dopant) are transported to the substrate regions.
- They are transferred to the substrate surface where they are absorbed.
- The chemical reaction occurs, followed by the growth of the epitaxial layer.
- The produces gases are desorbed.
- The reaction product are transported out from the reactor.
Molecular beam epitaxy (MBE)

- Thermal beams of atoms or molecules produced in evaporators condense on a crystalline surface under ultra high vacuum ($10^{-8}$ Pa)
- The result is a single crystal structure with thickness control of one atomic layer and precise doping concentration
Molecular beam epitaxy (MBE)
Film growth and deposition

- Thermal oxidation
  - gate thin oxide
  - surface thick oxide
- Dielectric deposition
  - inter-metal insulation
- Polysilicon deposition
  - gates and local interconnections
- Metallization
  - interconnections and pads
Thermal oxidation of Silicon

• Used to grow films of SiO₂ on the Si substrate surface

• Key factor in determining the success of Si technology
  – naturally grown by Si oxidation
  – good quality Si/SiO₂ interface
  – low impurity and defect concentration in SiO₂

• Dry oxidation
  – Si (solid) + O₂(gas) ⇌ SiO₂ (solid)

• Wet oxidation (with water vapor – much faster!)
  – Si (solid) + 2H₂O (gas) ⇌ SiO₂ (solid) + 2H₂ (gas)
Thermal oxidation of Silicon

- Furnace: quartz tube at high temperature: from 850°C to 1100°C
- The reaction rate follows an Arrhenius law:
  \[ v \approx A \exp\left(-\frac{E_a}{kT}\right) \quad E_a = \text{Activation energy [eV]} \]
Oxide growth law

- During the oxidation, part of the silicon reacts and is consumed
  - SiO$_2$: $2.2 \times 10^{22}$ molecules/cm$^3$
  - Si: $5 \times 10^{22}$ atoms/cm$^3$
  - Then, the consumed silicon thickness is 0.44 times the thickness of the formed SiO$_2$
Oxide growth law

• Three phases:
  (1) transfer of the reactants to the SiO$_2$
  (2) diffusion of reactants through formed SiO$_2$
  (3) reaction with the Si

F(1) = gas flux at the surface
F(2) = diffusion through SiO$_2$
F(3) = reaction rate at the SiO$_2$/Si
C$_0$ = oxidant species concentration at the surface
C$_i$ = oxidant species concentration at the SiO$_2$/Si interface
Oxide growth law

1. Transfer of the reactants to the SiO$_2$

\[ F(1) = h \cdot (C^* - C_0) \]

- $F(1)$ = gas flux at the surface
- $h$ = mass transfer coefficient in gaseous phase
- $C^*$ = oxidant species concentration at equilibrium in the oxide
- $C_0$ = oxidant species concentration at the surface

Basic model for the thermal oxidation of silicon
Oxide growth law

2. Diffusion through the formed SiO$_2$

\[ F(2) = D \cdot \frac{(C_0 - C_i)}{x_{ox}} \]

- $D$ = diffusivity
- $x_{ox}$ = oxide thickness
- $(C_0 - C_i)/x_{ox}$ = concentration gradient in the SiO$_2$

Basic model for the thermal oxidation of silicon
Oxide growth law

3. Oxidation reaction rate at the SiO$_2$/Si interface:

$$F(3) = k_S \cdot C_i$$

- $k_S = $ surface reaction rate

Basic model for the thermal oxidation of silicon
Oxide growth law

• At steady state:

\[ F(1) = F(2) = F(3) = F \]

• thus

\[ h \cdot \left( C^* - C_0 \right) = D \frac{(C_0 - C_i)}{x_{OX}} = k_s \cdot C_i \]

• starting from

\[ D \frac{(C_0 - C_i)}{x_{OX}} = k_s \cdot C_i = F \Rightarrow C_i = F / k_s \]

\[ \Rightarrow F = \frac{D \cdot C_0}{x_{OX} + D/k_s} \]
Oxide growth law

• Then, using

\[ h \cdot \left( C^* - C_0 \right) = F \Rightarrow C^* - \frac{F}{h} = C_0 \]

\[ \Rightarrow F = \frac{D \cdot \left( C^* - \frac{F}{h} \right)}{x_{OX} + D/k_s} \]

• Solving for F

\[ F = \frac{k_s \cdot C^*}{1 + k_s/h + x_{OX} \cdot k_s/D} \]
Oxide growth law

• Growth rate $R$ (thickness per unit time) given by ratio of flux $F$ over number of oxidizing molecules required to form a unit volume of SiO$_2$:
  
  – $2.2 \times 10^{22}$ molecules/cm$^3$ of SiO$_2$
  
  – $N_{ox} = 2.2 \times 10^{22}$ cm$^{-3}$ of O$_2$ molecules required for dry oxidation

   OR

  – $N_{ox} = 4.4 \times 10^{22}$ cm$^{-3}$ of H$_2$O molecules required for wet oxidation

• Then

$$R = \frac{dx_{ox}}{dt} = \frac{F}{N_{ox}} = \frac{k_s \cdot C^*}{N_{ox} \cdot (1 + k_s/h + x_{ox} \cdot k_s/D)}$$
Oxide growth law

- The differential equation can be solved for $x_{ox}(t)$:

$$\int \left[ D \left( \frac{1}{k_s} + \frac{1}{h} \right) + x_{ox} \right] dx_{ox} = \frac{D \cdot C^*}{N_{ox}} dt_{ox}$$

$$x_{ox}^2 + A \cdot x_{ox} = B \cdot (t_{ox} + \tau)$$

- where

$$A = 2 \cdot D \left( \frac{1}{k_s} + \frac{1}{h} \right), \quad B = \frac{2 \cdot D \cdot C^*}{N_{ox}}$$

$$\tau = \frac{x_{ox}^2}{B} + \frac{x_{ox}}{B/A} \quad \text{time shift due to initial oxide thickness}$$
Oxide growth law

\[ x_{\text{ox}}(t) = \frac{A}{2} \left[ \sqrt{1 + \frac{(t + \tau)}{A^2/4 \cdot B}} - 1 \right] \]

- Short times: growth limited by surface reaction speed
  \[ x_{\text{ox}}(t) \approx \frac{B}{A} \cdot (t + \tau) \]

- Long times: growth limited by diffusion through SiO\textsubscript{2}
  \[ x_{\text{ox}}(t) \approx \sqrt{B \cdot (t + \tau)} \approx \sqrt{B \cdot t} \]
Oxide growth law

\[
\frac{B/A}{B} = D_0 \cdot \exp\left(-\frac{E_A}{kT}\right)
\]

choose appropriate value of \(D_0\) from the table below

| Table 3.1 Values for Coefficient \(D_0\) and Activation Energy \(E_A\) for Wet and Dry Oxygen.* |
|---|---|---|---|---|
| Wet \(O_2\) \((X_i = 0 \text{ nm})\) & Dry \(O_2\) \((X_i = 25 \text{ nm})\) & | | |
| \(D_0\) & \(E_A\) & \(D_0\) & \(E_A\) & |
| \(\langle 100 \rangle \text{ Silicon}\) & | | |
| Linear \((B/A)\) & \(9.70 \times 10^7 \mu\text{m/hr}\) & 2.05 eV & \(3.71 \times 10^6 \mu\text{m/hr}\) & 2.00 eV |
| Parabolic \((B)\) & \(386 \mu\text{m}^2/\text{hr}\) & 0.78 eV & \(772 \mu\text{m}^2/\text{hr}\) & 1.23 eV |
| \(\langle 111 \rangle \text{ Silicon}\) & | | |
| Linear \((B/A)\) & \(1.63 \times 10^8 \mu\text{m/hr}\) & 2.05 eV & \(6.23 \times 10^6 \mu\text{m/hr}\) & 2.00 eV |
| Parabolic \((B)\) & \(386 \mu\text{m}^2/\text{hr}\) & 0.78 eV & \(772 \mu\text{m}^2/\text{hr}\) & 1.23 eV |

*Data from ref. [7].
Oxide growth law

Linear rate constant $B/A$

Parabolic rate constant $B$

$T$ (°C)

$T$ (°C)

Dry $\text{O}_2 (10^5 \text{ Pa})$
$E_a = 2.0 \text{ eV}$

(111) Si
(100) Si

Wet oxidation
$\text{H}_2\text{O} (10^5 \text{ Pa})$
$E_a = 0.71 \text{ eV}$

Dry oxidation
$\text{O}_2 (10^5 \text{ Pa})$
$E_a = 1.24 \text{ eV}$

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Oxide growth law

- **Dry oxidation**
  - (111)
  - (100)

- **Wet oxidation**
  - (111)
  - (100)

Graphs showing oxide thickness as a function of oxidation time at different temperatures for wet and dry oxidation.
Thin (gate) and thick oxide

- Micrograph of a cross-section of an active region bounded by LOCOS

- gate thin oxide
- thick oxide to isolate MOSFET's
- p-Si substrate
Trench isolation

- Used in modern CMOS technologies ($L \leq 250$ nm) instead of LOCOS
- Trenches etched between devices and filled with dielectric material
  - dielectric deposition technique required
Inter-layer dielectric (ILD)

- metal7
- metal6
- metal5
- metal4
- metal3
- metal2
- metal1

MOSFET region

inter-metal dielectric

via connecting metal n to metal n-1
Inter-layer dielectric (ILD)

- Materials used for ILD
  - $\text{SiO}_2$ ($\varepsilon_{\text{ox}} = 3.9$, used in CMOS processes $\geq 250 \text{ nm}$)
  - low-k materials ($\varepsilon_{\text{lk}} \approx 2$, used to reduce interconnect parasitic capacitance in CMOS processes $\leq 180 \text{ nm}$)
Inter-layer dielectric (ILD)

- ILD realization techniques
  - Chemical vapor deposition (CVD)
  - Quality of deposited SiO$_2$ worse than that of thermally grown SiO$_2$ ⇒ used as ILD, doping mask or to increase thickness of thermal oxide
Polysilicon deposition

- Polycrystalline Silicon (polysilicon) used for
  - MOSFET's gates in technologies $1 \mu m \geq L \geq 65$ nm
  - local interconnections
  - integrated capacitor plates

- Realized by deposition
  - thermal decomposition of Silane ($SiH_4$) in a low pressure reactor at $580 \div 650$ °C

  $SiH_4 \leftrightarrow Si + 2H_2$
Metallization

• Aluminum metallization for interconnects
  – used until late 90's
  – blanket deposition, then selectively etched to form desired interconnection patterns
  – problems: electromigration, spiking, resistivity

• Copper (double) damascene technology
  – lower resistivity than Al (1.7÷2 vs 2.7÷3 Ωcm)
  – better resistance to electromigration
  – problems: difficult to pattern using standard etching techniques
  – solution: damascene process
Damascene process

- Metal deposition and PR pattern definition
- Metal etching according to PR pattern
- Dielectric deposition
- Etching of excess dielectric
- Dielectric deposition and PR pattern definition
- Etching of trenches for metal lines
- Trenches filled by metal deposition
- Excess metal removed by planarization
- Deposition of dielectric upper layer
Damascene process in detail

1. Etch and Deposit Barrier Layer
   - Copper must be encapsulated to prevent out-diffusion
2. Electroplating
3. CMP
   - Copper connections between tungsten plugs
4. Deposit Seed Layer

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Doping

- Doping is the process by means of which selected impurities are inserted in a semiconductor substrate.
- Impurities can be of acceptor or donor type and must be in a substitutional position to be active.
- Main dopants for Silicon:

<table>
<thead>
<tr>
<th>Element</th>
<th>Group</th>
<th>Type</th>
<th>Carriers</th>
</tr>
</thead>
<tbody>
<tr>
<td>B</td>
<td>III</td>
<td>P</td>
<td>Holes</td>
</tr>
<tr>
<td>P</td>
<td>V</td>
<td>N</td>
<td>Electrons</td>
</tr>
<tr>
<td>As</td>
<td>V</td>
<td>N</td>
<td>Electrons</td>
</tr>
</tbody>
</table>

- Main Technologies:
  - Predeposition + Diffusion
  - Ionic implantation + Recrystallization + diffusion
Doping by diffusion

- Predeposition of a fixed amount of dopant in a thin surface layer
- Diffusion (drive-in) of dopant into the substrate
  - depth of diffusion controlled by drive-in temperature and time

![Diagram of doping by diffusion](image)
Doping by diffusion

\[ \text{Ln(C)} \]

Predeposition

\[ \text{erfc} \]

Diffusion \( t_1 \)

Diffusion \( t_2 > t_1 \)

Gaussian
Doping by diffusion

- Predeposition with constant dopant concentration $C_S$ at the surface

$$N(x,t) = C_S \text{erfc} \left( \frac{x}{\sqrt{4Dt}} \right)$$

pre-doping profile at time $t$

$$N' = Q = 2C_S \sqrt{\frac{Dt}{\pi}}$$

amount of dopant inserted into substrate at time $t$

- Drive-in of a fixed amount $N'$ of dopant

$$N(x,t) = \frac{Q}{\sqrt{\pi Dt}} \exp \left( - \frac{x^2}{4Dt} \right)$$

doping profile at time $t$

$$N(0,t) = \frac{Q}{\sqrt{\pi Dt}}$$

surface doping level at time $t$
Doping by ion implantation

• Dopant ions shot by an ion gun at $10 \div 1000$ KeV
• Ions penetrate into substrate and lose kinetic energy to lattice atoms
• Patterned oxide acts as mask so that dopant is implanted in selected substrate regions

P-Si
Doping by ion implantation

• Ions that enter into the substrate are subject to random inelastic interactions with lattice atoms
  – resulting doping profile shows a Gaussian shape
Doping by ion implantation

Figure 4-61. Masking Thickness Required, Boron and Antimony Implants.

Figure 4-62. Diagrammatic Representation of an Ion Implanter.
Doping by ion implantation

• High-energy ions cause severe crystal damage
• A re-adjustment of the crystal is required through a thermal annealing step
• Thermal annealing causes a dopant redistribution (due to a diffusion mechanisms) and this is an unwanted effect
  – RTA (rapid thermal annealing): high temperatures (1000 °C) for short time (10 sec) limits dopant redistribution
Doping by ion implantation

Doping profile after implant

\[ C(x) = C_p \cdot \exp \left( -\frac{(x - R_p)^2}{2 \cdot \Delta R_p^2} \right) \]

\[ C_p = \frac{N'}{\sqrt{2\pi\Delta R_p}} \]

- \( N' \) (or Q) = implanted dose
- \( C_p \) = concentration peak
- \( L = \sqrt{2 \cdot \Delta R_p} \) = Gaussian width
Doping by ion implantation

- Two parameters
  - \( R_p \): projected range
  - \( \Delta R_p \): standard deviation
  - both depend on ion energy, ion type, substrate material

- See MK book for implantation data:
  - fig. 2.16 (Boron)
  - fig. 2.17 (Phosphorus)
  - fig. 2.18 (Arsenic)
Doping by ion implantation

• Annealing increases Gaussian width due to diffusion of dopant:

\[ N(x) = \frac{Q}{L' \sqrt{\pi}} \exp \left[ -\left( \frac{x - R_p}{L'} \right)^2 \right] \]

\[ L' = \sqrt{2 \Delta R_p^2 + 4Dt} \]
Doping by ion implantation

Before annealing

After annealing