Progettazione e sintesi di circuiti digitali

Lecture 4
Timing constraints in synchronous sequential systems
Basic storage elements

- **Latch**: memory element sensitive to the level of an enable signal
  - transparent when E high (low), state stored when E low (high)
- **Flip-flop**: memory element sensitive to the edge of a clock signal
  - never transparent, state changes based on input value at rising (falling) edge of CLK

![Positive D latch circuit diagram](image1)

![Positive-edge-triggered D flip-flop circuit diagram](image2)

*positive D latch*

*positive-edge-triggered D flip-flop*
Static D latch

- Can be realized using a transmission gate multiplexer and inverters
Static D flip-flop

Master-slave configuration of two D latches enabled on opposite CLK phases
Timing metrics in registers

- **setup time** ($t_{su}$ or $t_s$): time that the input data must be valid and stable before the clock edge
- **hold time** ($t_{hold}$ or $t_h$): time that the input data must remain valid and stable after the clock edge
- **propagation delay** ($t_{PCQ}$ or $t_{C-Q}$): time after the clock edge when the output data is stable and valid
Timing metrics in combinational circuits

- **propagation delay** ($t_{pAY}$ or $t_{dAY}$): time from the last input signal change until the last output signal change
  - Also: input at steady state to output at steady state
- **contamination delay** ($t_{cAY}$): time from the first input signal change to the first output signal change
  - Also: input contaminated to output contaminated
Timing constraints in synchronous systems

- Data are launched by a register and are captured by a register

```latex
\begin{align*}
\begin{cases}
t_{pCQ} + t_{pQA} + t_{su} & \leq T_{CLK} \\
t_{cCQ} + t_{cQA} & \geq t_{hold}
\end{cases}
\end{align*}
```

- setup time constraint
  - sets maximum propagation delays or minimum clock period
- hold time constraint
  - sets minimum contamination delays
Timing constraints in synchronous systems

- Launching or capturing register sometimes are not part of the circuit being designed

\[
\begin{align*}
\text{hold}_{cAB} & \geq t_{\text{hold}} \\
\text{hold}_{cIN} & \geq t_{\text{hold}}
\end{align*}
\]

\[
\begin{align*}
t_{\text{pIN}} + t_{\text{pAB}} + t_{\text{su}} & \leq T_{\text{CLK}} \\
t_{\text{cIN}} + t_{\text{cAB}} & \geq t_{\text{hold}}
\end{align*}
\]

circuit being designed

details unknown or not yet defined

estimate (or guess) of propagation and contamination delays
Timing constraints in synchronous systems

- Launching or capturing register sometimes are not part of the circuit being designed

\[
\begin{align*}
  t_{pCQ} + t_{pQA} + t_{pOUT} & \leq T_{CLK} \\
  t_{cCQ} + t_{cQA} + t_{cOUT} & \geq t_{hold}
\end{align*}
\]
Timing constraints in FSM

\[
\begin{align*}
\max(t_{pIN}, t_{pREG}) + t_{pCOMB} + \max(t_{su}, t_{pOUT}) & \leq T_{CLK} \\
\min(t_{cIN}, t_{cREG}) + t_{cCOMB} & \geq t_{hold}
\end{align*}
\]
Timing constraints example

\[ t_{PCQ} = t_{CCQ} = t_s = 150\text{ps} \]
\[ t_h = 250\text{ps} \]
\[ t_{pMax} = 850\text{ps} \]
\[ t_{cMin} = 100\text{ps} \]

Is hold time constraint met?

What is the minimum cycle time?
Clock skew

- What if clock edges are not exactly synchronous at different registers?

Statistical variable due to differences in wires and buffers propagation delays

\[
\begin{align*}
\begin{cases}
t_{pCQ} + t_{pQA} + t_{su} + t_{sk} & \leq T_{CLK} \\
t_{cCQ} + t_{cQA} - t_{sk} & \geq t_{hold}
\end{cases}
\]

clock skew tightens the timing constraints